WHAT IS CLAIMED IS:

1. A method for programming and verifying data in a programmable circuit, the method comprising:

shifting first data bits into first registers;

loading second data bits from first memory cells into the first registers, the first memory cells being in a first word line selected by first address bits in second registers; and

loading the first data bits into second memory cells, the second memory cells being in a second word line selected by the first address bits.

2. The method of claim 1 further comprising:

storing the first data bits using a first set of latches after the first data bits are shifted into the first registers, and wherein the first data bits are loaded into the second memory cells from the first set of latches.

3. The method of claim 2 further comprising:

storing the first data bits using a second set of latches after the first data bits are stored using the first set of latches, each of the second set of latches being coupled to a multiplexer.

4. The method of claim 3 further comprising:

for each of the multiplexers,

selecting a first signal for loading the second data bits from the first memory cells into the first registers or a second signal for loading third data bits from the first memory cells into the first registers.

5. The method of claim 1 wherein loading the second data bits from the first memory cells into the first registers further comprises:

loading a first subset of the second data bits that have a first logic state from the first memory cells into the first registers in response to a first verify control signal, and loading a second subset of the second data bits that have a second logic state from the first memory cells into the first registers in response to a second verify control signal.

6. The method of claim 1 wherein the first word line is adjacent to the second word line, and the first address bits select the first and second word lines using a multiplexer that is responsive to a verify control signal.

7. The method of claim 1 further comprising:

shifting the second data bits out of the first registers while shifting third data bits into the first registers.

8. The method of claim 7 further comprising:

loading the first data bits from the second memory cells into the first registers, the second memory cells being in the second word line selected by second address bits in the second registers; and

loading the third data bits into third memory cells, the third memory cells being in a third word line selected by the second address bits.

9. The method of claim 8 wherein loading the first data bits from the second memory cells into the first registers further comprises:

loading a first subset of the first data bits from the second memory cells into the first registers in response to a first verify control signal, and loading a second subset of the first data bits from the second memory cells into the first registers in response to a second verify control signal.

10. A programmable circuit comprising:

a plurality of memory cells arranged in rows and columns;

first registers, each of the first registers being coupled to one of the rows of memory cells through interconnection conductors, first address bits being stored in the first registers; and

second registers, each of the second registers being coupled to one of the columns of memory cells through interconnection conductors, first data bits stored in a first row of the memory cells being loaded into the second registers when the first row is selected by the first address bits, and second data bits stored in the second registers being programmed into a second row of the memory cells when the second row is selected by the first address bits.

11. The programmable circuit of claim 10 wherein each of the first registers is coupled to two rows of the memory cells through a multiplexer circuit.

12. The programmable circuit of claim 10 wherein each of the second registers is coupled to a first latch that stores the second data bits before the second data bits are programmed into the second row of the memory cells.

13. The programmable circuit of claim 12 wherein each of the first latches is coupled to a second latch that stores one of the second data bits,

each of the second latches being coupled to the select input of a multiplexer that selects a first verify control signal or a second verify control signal.

14. The programmable circuit of claim 13 wherein a first subset of the first data bits having a first logic state are loaded into the second registers in response to the first verify control signal, and a second subset of the first data bits having a second logic state are loaded into the second registers in response to the second verify control signal.

15. The programmable circuit of claim 10 further comprising:

an ISC control block that provides a program signal and a verify signal,

wherein the second data bits stored in the second registers are programmed into the second row of the memory cells in response to the program signal, and

the first data bits stored in the first row of the memory cells are loaded into the second registers in response to the verify signal.

16. The programmable circuit of claim 10 wherein second address bits stored in the first registers select the second row of the memory cells and a third row of the memory cells, and

the second data bits stored in the second row of the memory cells are loaded into the second registers when the second row is selected by the second address bits, and third data bits stored in the second registers are programmed into the third row of the memory cells when the third row is selected by the second address bits.

17. The programmable circuit of claim 16 wherein third address bits stored in the first registers select the third row of the memory cells and a fourth row of the memory cells, and

the third data bits stored in the third row of the memory cells are loaded into the second registers when the third row is selected by the third address bits, and fourth data bits stored in the second registers are programmed into the fourth row of the memory cells when the fourth row is selected by the third address bits.

18. The programmable circuit of claim 17 wherein fourth address bits stored in the first registers select the fourth row of the memory cells, and

the fourth data bits stored in the fourth row of the memory cells are loaded into the second registers when the fourth row is selected by the fourth address bits.

19. A programmable circuit comprising:

means for selecting a first row and a second row of memory cells using first address bits;

means for verifying first data programmed into the first row of memory cells; and

means for programming second data into the second row of memory cells.

20. The programmable circuit of claim 19 wherein the means for verifying the first data programmed into the first row of memory cells further comprises:

means for verifying a first subset of the first data at a first logic state; and

means for verifying a second subset of the first data at a second logic state.

21. The programmable circuit of claim 19 wherein the means for selecting the first row and the second row of memory cells further comprises:

a first register coupled to the first and second rows of memory cells through a multiplexer, wherein the first address bits are stored in the first register for selecting the first row and the second row of memory cells using the multiplexer.

22. The programmable circuit of claim 19 wherein the means for programming the second data into the second row of memory cells further comprises second registers, each of the second registers storing the second data in latches before the second data is programmed into the second row of memory cells.

23. The programmable circuit of claim 19 further comprising:

means for selecting the second row and a third row of memory cells using second address bits;

means for verifying the second data programmed into the second row of memory cells; and

means for programming third data into the third row of memory cells.

24. The programmable circuit of claim 23 further comprising:

means for selecting the third row and a fourth row of memory cells using third address bits;

means for verifying the third data programmed into the third row of memory cells; and

means for programming fourth data into the fourth row of memory cells

25. A method for programming and verifying data in a programmable circuit, the method comprising:

shifting first data bits into first registers;

loading second data bits from first memory cells in a first word line into the first registers;

loading the first data bits into second memory cells in a second word line;

shifting third data bits into the first registers while shifting the second data bits out of the first registers; and

loading the third data bits into third memory cells in a third word line.

26. The method of claim 25 further comprising:

loading the first data bits from the second memory cells into the first registers; and

shifting fourth data bits into the first registers while shifting the first data bits out of the first registers.

27. The method of claim 26 wherein loading the second data bits from the first memory cells into the first registers comprises selecting the first word line with first address bits in second registers;

and wherein loading the first data bits into second memory cells in the second word line comprises selecting the second word line with the first address bits in the second registers.

28. The method of claim 27 wherein loading the first data bits from the second memory cells into the first registers comprises selecting the second word line with second address bits in the second registers; and

wherein loading the third data bits into the third memory cells comprises selecting the third word line with the second address bits in the second registers.

29. A programmable circuit comprising:

a plurality of memory cells arranged in rows and columns;

a first plurality of registers, each of the registers being coupled to one of the columns of memory cells through interconnection conductors, wherein first data bits stored in a first row of the memory cells are loaded into the first registers; and

a first plurality of latches, each of the latches being coupled to one of the first plurality of registers, wherein the first data bits are shifted out of the first registers while second data bits are shifted into the first registers, the second data bits being stored in the first plurality of latches and programmed into a second row of the memory cells.

30. The programmable circuit of claim 29 wherein the first row of the memory cells and the second row of the memory cells are selected by address bits in second registers, each of the second registers being coupled to one of the rows of memory cells through interconnection conductors.